

500kHz 7A High Efficiency Synchronous PWM Boost Converter



General Description

The FP6277 is a current mode boost DC-DC converter with PWM/PSM control. Its PWM circuitry with built-in 30mΩ high side switch and 30mΩ low side switch make this regulator highly power efficient. The internal compensation network also minimizes external component counts to only 6. An internal 0.6V voltage is connected to error amplifier the non-inverting input as precision reference voltage. Built-in soft-start function can reduce the inrush current.

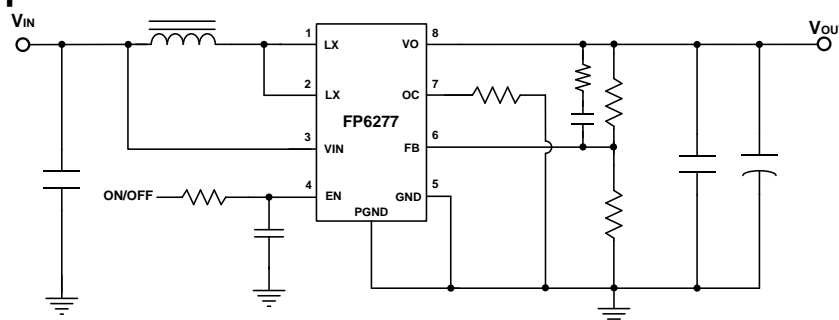
Features

- Current mode with PWM/PSM control
- Input voltage range: 2.4V~4.5V
- Adjustable Output up to 5.3V
- Shutdown current: <1uA
- Oscillator frequency: 500KHz
- Reference voltage: 0.6V +/-2%
- Disconnect load during shutdown
- Cycle-by-cycle current limit
- Low $R_{DS(on)}$: 30mΩ for both high and low side
- Protection: OTP, OCP, SCP
- Internal compensation
- Internal soft-start: 7ms
- Package: SOP-8L(EP)

Applications

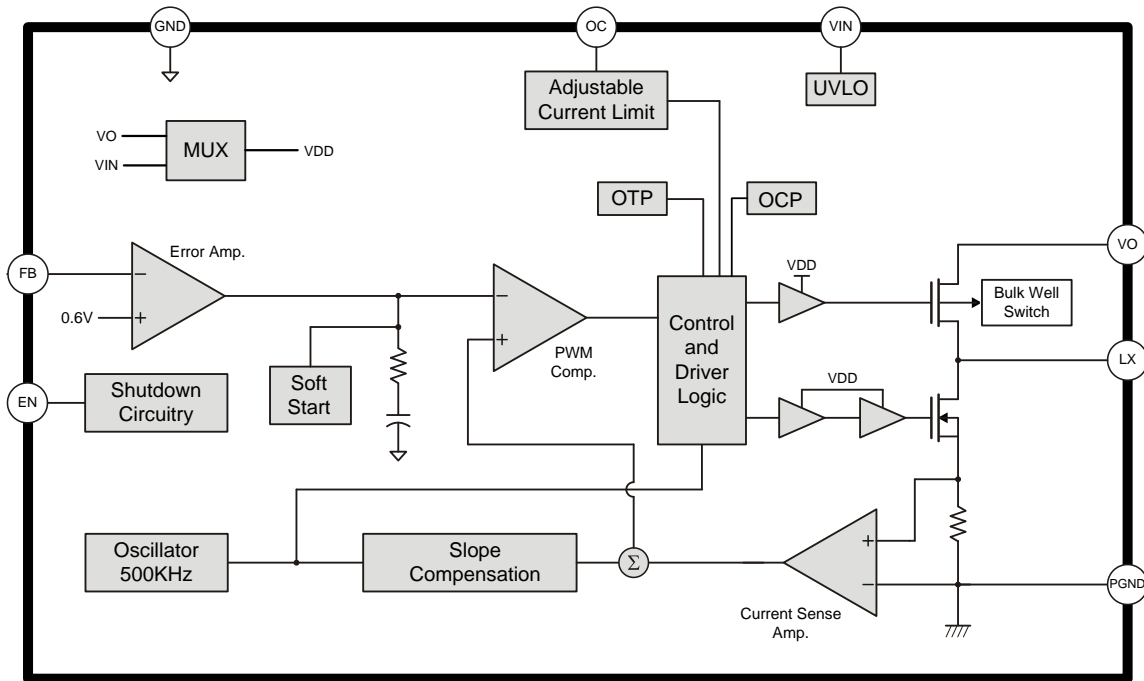
- Chargers
- Handheld Devices
- Portable Products
- Power Bank

Typical Application Circuit



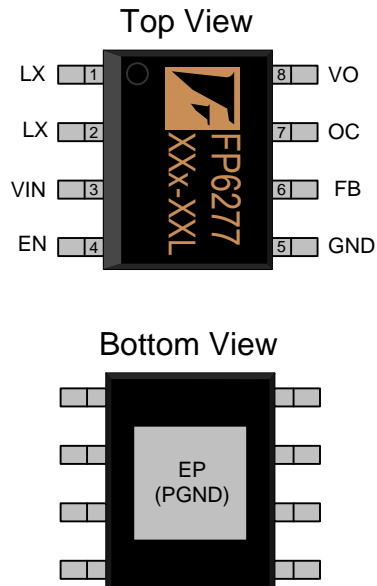
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Function Block Diagram



Pin Descriptions

SOP-8L (EP)

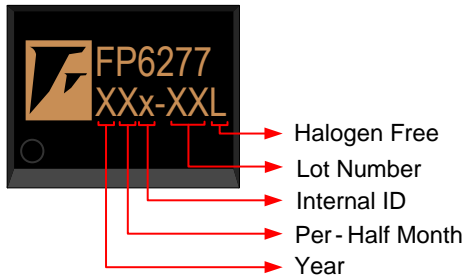


Name	No.	I / O	Description
LX	1	I	Power Switch Output
LX	2	I	Power Switch Output
VIN	3	P	IC Power Supply
EN	4	I	Enable Control (Active High)
GND	5	P	IC Ground
FB	6	I	Error Amplifier Inverting Input
OC	7	I	Adjustable Current Limit (The resistor must be connected to ground.)
VO	8	O	Output Voltage Pin
PGND	EP	P	IC Power Ground (Must connect to GND)

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Marking Information

SOP-8L(EP)



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example → Lot : 123456 → XXx-56L

Internal ID: Internal Identification Code

Per-Half Month: Production period indicator in half-month time unit

For Example : A → First Half Month of January
B → Second Half Month of January
C → First Half Month of February
D → Second Half Month of February

Year: Production year's last digit

Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP6277XR-G1	-40°C ~ 85°C	SOP-8L(EP)	2500EA	Tape & Reel

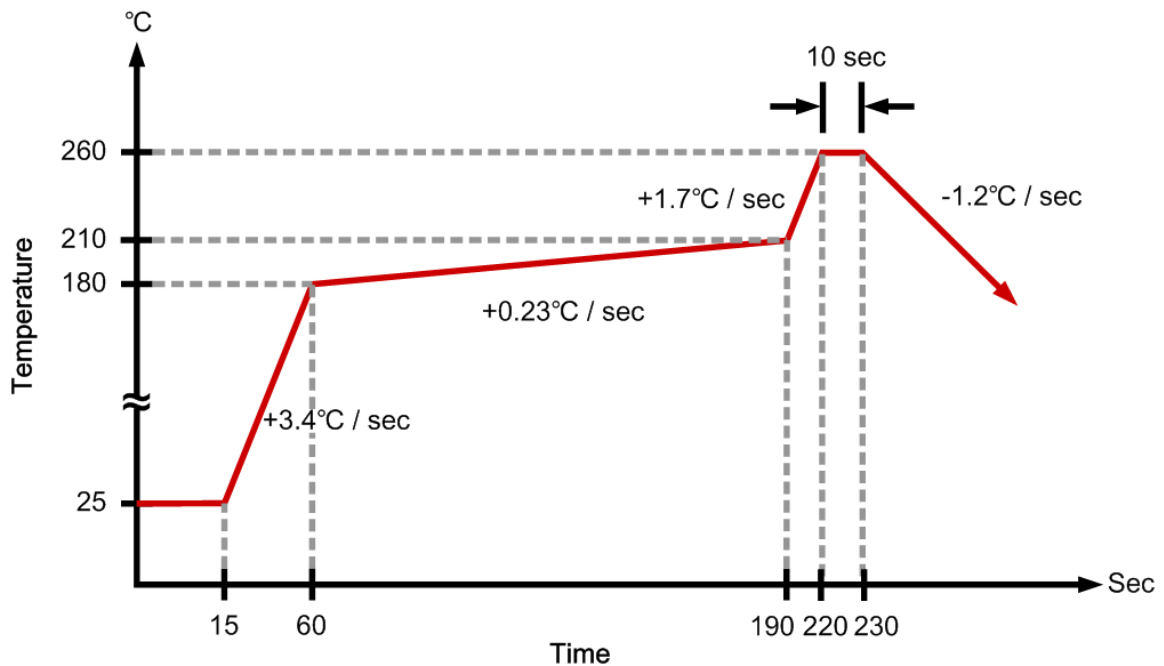
Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}		0		6	V
LX Voltage	V_{LX}		0		7	V
EN,FB,OC,VO Voltage			0		6	V
Thermal Resistance (Note1)	θ_{JA}	SOP-8L(EP)			+60	°C / W
Junction Temperature	T_J				+150	°C
Operating Temperature	T_{OP}		-40		+85	°C
Storage Temperature	T_{ST}		-65		+150	°C
Lead Temperature		(soldering, 10 sec)			+260	°C

Note1:

θ_{JA} is measured in the natural convection at $T_A=25^\circ\text{C}$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}		2.4		4.5	V
Operating Temperature Range	T_A	Ambient Temperature	-40		+85	°C

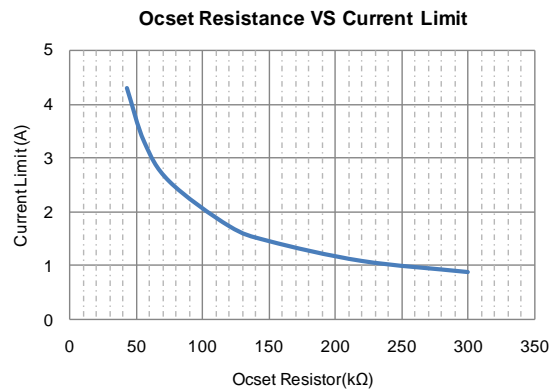
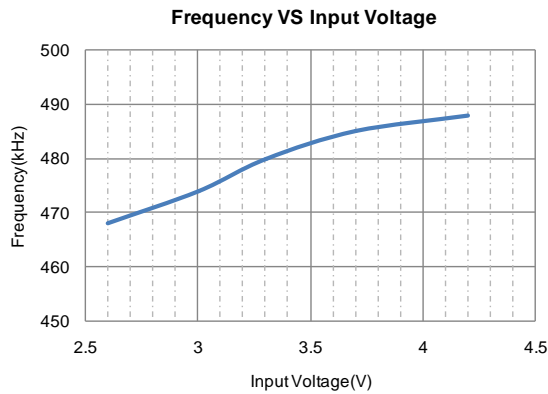
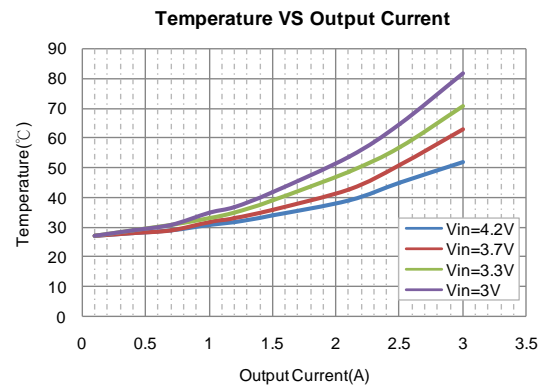
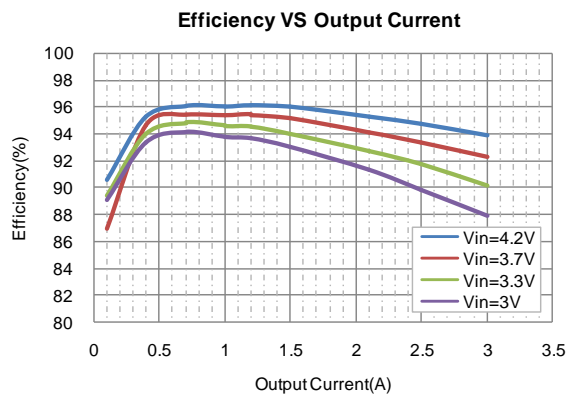
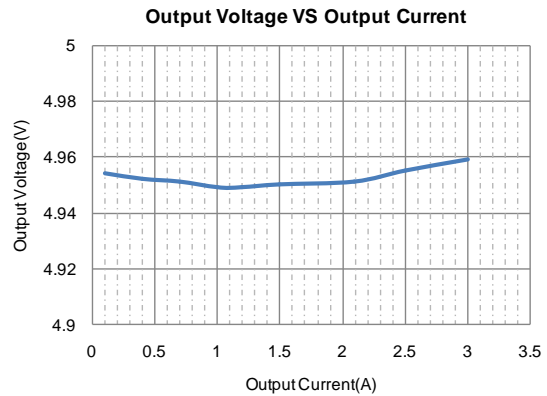
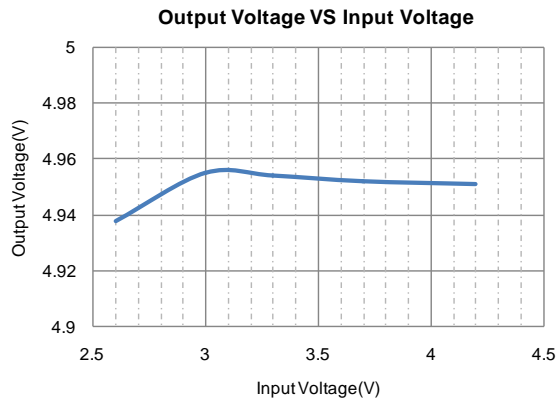
DC Electrical Characteristics ($V_{IN}=3.3V$, $T_A=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}		2.4		4.5	V
Under Voltage Lockout	V_{UVLO}			2.1		V
UVLO Hysteresis				0.1		V
Quiescent Current	I_{CC}	$V_{FB}=0.65V$, No switching		280		μA
Average Supply Current	I_{CC}	$V_{FB}=0.55V$, Switching		3.6		mA
Shutdown Current	I_{CC}	$V_{EN}=GND$		0.1		μA
Linear Charge Current	I_{CHARGE}	$V_{OUT}<V_{IN}$	4.5			A
Operation Frequency	f_{OSC}	$V_{FB}=0.55V$		500		kHz
Maximum Duty Ratio	%			90		%
Feedback Voltage	V_{REF}	$V_{IN}=4.5V$	0.588	0.6	0.612	V
Enable Voltage	V_{EN}		0.96			V
Shutdown Voltage	V_{EN}				0.6	V
Soft-Start Time	t_{SS}	$V_{IN}=4.5V$		7		ms
High Side Switch $R_{DS(ON)}$	$R_{ON-PMOS}$			30		m Ω
Low Side Switch $R_{DS(ON)}$	$R_{ON-NMOS}$			30		m Ω
Internal Switch Current Limit	I_{OCP}			7		A
Thermal Shutdown Threshold	T_{OTP}			150		°C
Thermal Shutdown Hysteresis				30		°C

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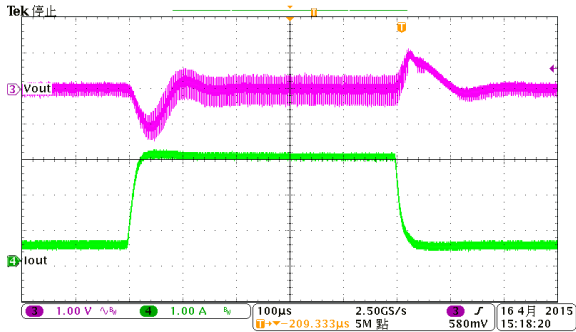
Typical Operating Characteristics

($V_{CC}=3V, V_{out}=5V, I_{out}=2.5A, T_A=25^{\circ}C$, unless otherwise specified)

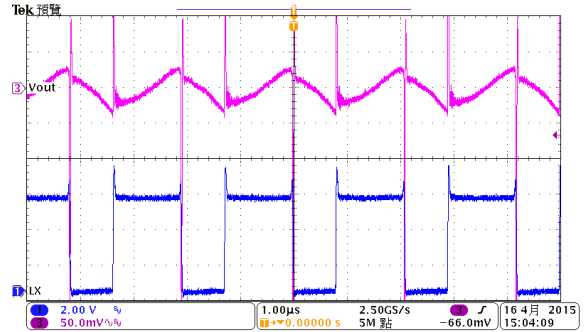


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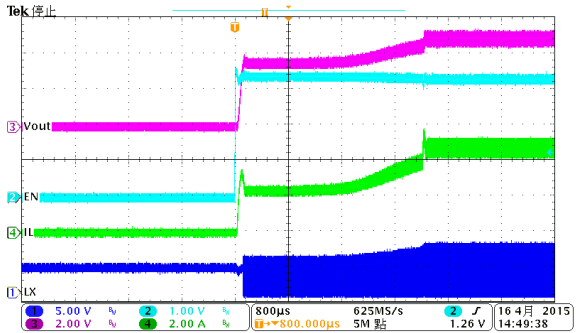
Transient Response
($V_{IN}=3.3V$, $V_{OUT}=5V$, $I_{OUT}=0.5\sim 3A$)



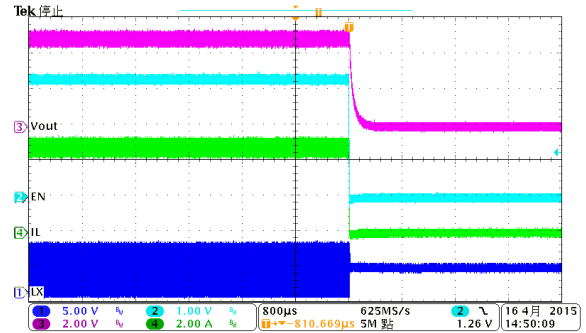
Output Ripple
($V_{IN}=3.3V$, $V_{OUT}=5V$, $I_{OUT}=3A$)



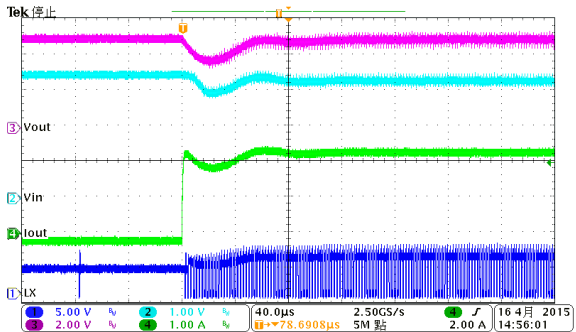
EN ON Test
($V_{IN}=3.3V$, $V_{OUT}=5V$, $I_{OUT}=3A$)



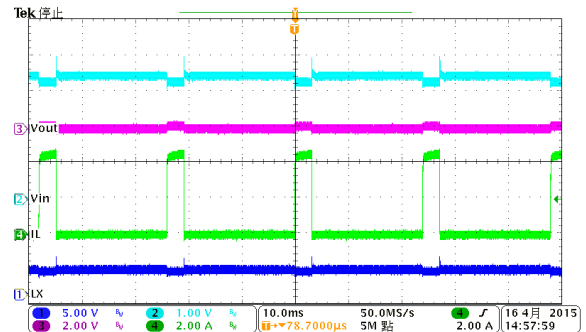
EN OFF Test
($V_{IN}=3.3V$, $V_{OUT}=5V$, $I_{OUT}=3A$)



Load ON Test
($V_{IN}=3.3V$, $V_{OUT}=5V$, $I_{OUT}=3A$)



Short Test
($V_{IN}=3.3V$, $I_{OUT}=3A$)



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Function Description

Operation

The FP6277 is a current mode synchronous boost converter. The constant switching frequency is 500 kHz and operates with pulse width modulation (PWM). Build-in 30mΩ high side switch and 30mΩ low side switch provides a high efficient conversion.

Soft Start Function

Soft start circuitry is integrated into FP6277 to avoid inrush current during power on. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current.

Current Limit Program

A resistor between OC and GND pin programs peak switch current. The resistor value should be between 26.5k and 300k. The current limit can be set from 7A to 0.8A. The OC pin can't float must connect a resistor to ground. Keep traces at this pin as short as possible. Do not put capacitance at this pin. Set the over current trip point according to the following equation:

$$I_{OCP} = \frac{180000}{R3} + 0.2$$

Over Temperature Protection (OTP)

FP6277 will turn off the power MOSFET automatically when the internal junction temperature is higher than 150°C. The power MOSFET wake up when the junction temperature drops 30°C under the OTP threshold temperature.

Application Information

Inductor Selection

Inductance value is decided based on different condition. 1.5uH to 4.7uH inductor value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency. Also, avoid inductor saturation which will cause circuit system unstable and lower core loss at 500KHz.

Capacitor Selection

The output capacitor is required to maintain the VO DC voltage. Low ESR capacitors are preferred to reduce the output voltage ripple. Ceramic capacitor of X5R and X7R are recommended, which have low equivalent series resistance (ESR) and wider operation temperature range.

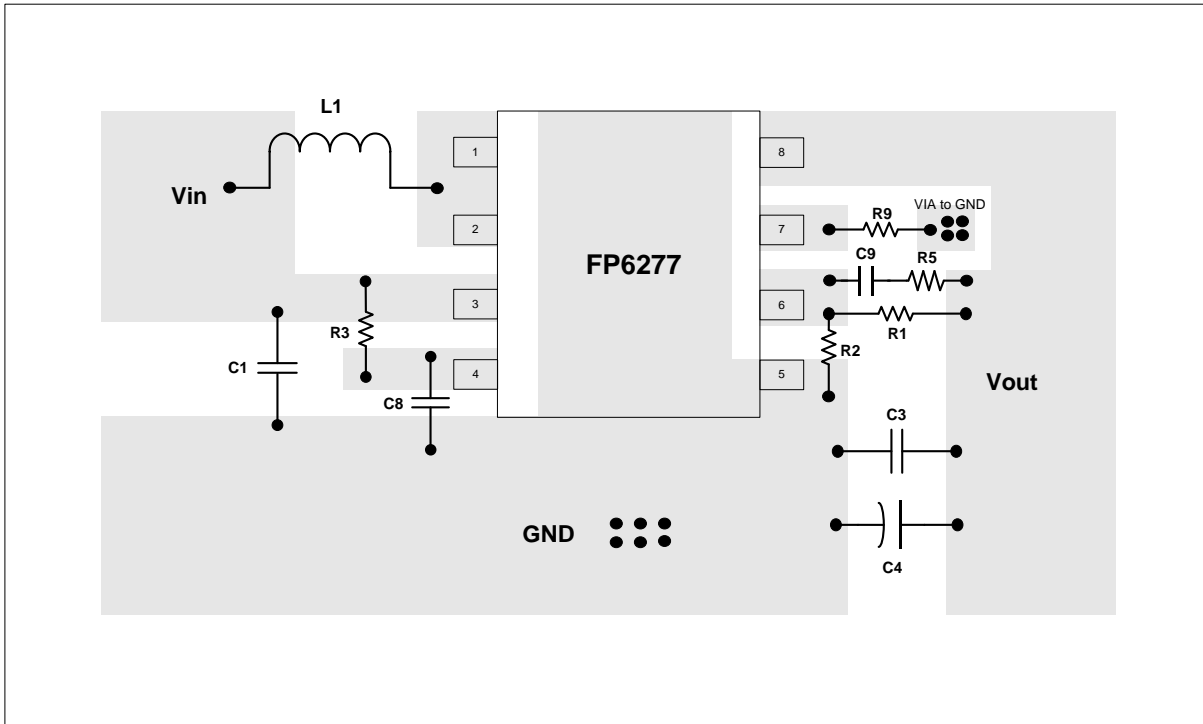
Output Voltage Programming

The output voltage is set by a resistive voltage divider from the output voltage to FB. The output voltage is:

$$V_{OUT} = 0.6V \left(1 + \frac{R1}{R2} \right)$$

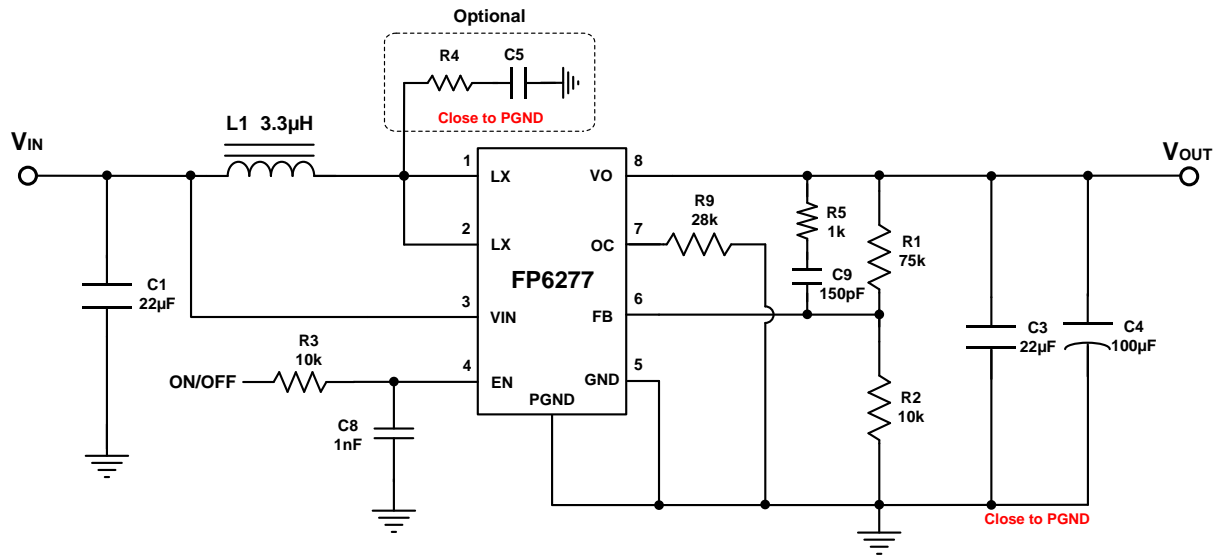
Layout Considerations

1. The power traces, consisting of the GND trace, the LX trace and the V_{IN} trace should be kept short, direct and wide.
2. Layout LX switching node wide and short trace to reduce EMI.
3. Place C1 near VIN pin as closely as possible to maintain input voltage steady and filter out the pulsing input current.
4. The resistive divider R1 and R2 must be connected to FB pin directly and as closely as possible.
5. FB is a sensitive node. Please keep it away from switching node LX.
6. The GND of the IC, C1, C3 and C4 should be connected close together directly to a power ground plane.



Suggested Layout

Typical Application

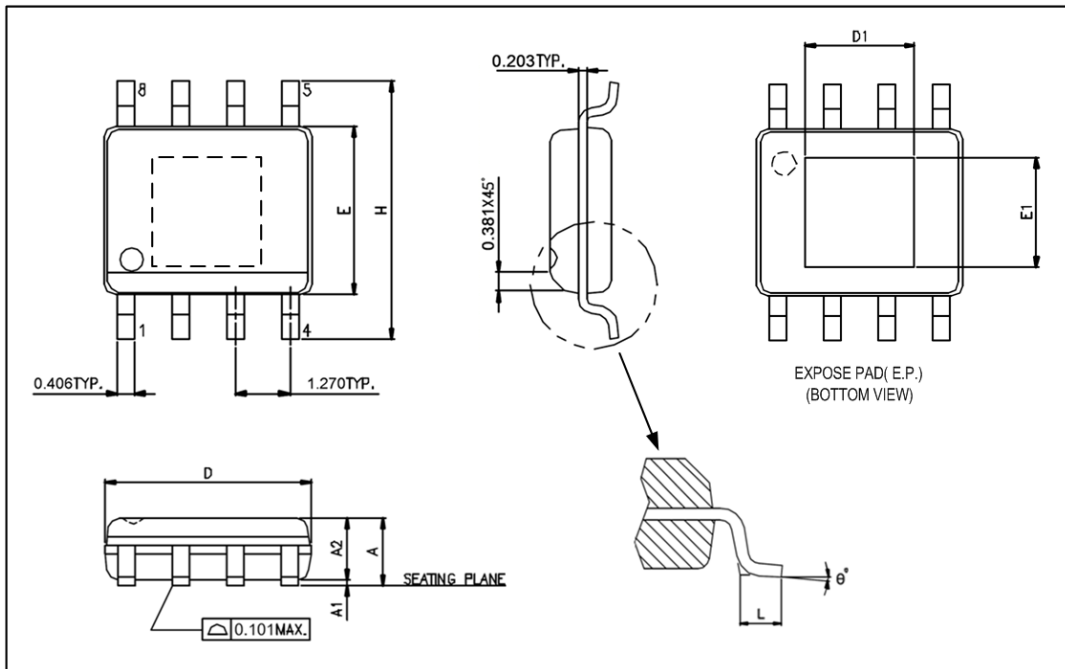


Note:

1. Use ceramic capacitor of X5R or X7R for C1 and C3.
2. R4 and C5 are added for reducing EMI (Electromagnetic Interference).
3. EN voltage must be less than or equal to VIN voltage.
4. The OC pin must connect a resistor R9 to ground setting current limit.

Package Outline

SOP-8L (EP)



Unit: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.050	0.152
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
D1		3.302 REF
E1		2.413 REF

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.
2. Dimension "D" does not include molding flash, protrusions or gate burrs.
3. Dimension "E" does not include inter-lead flash or protrusions.

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